Simple Noise Deembedding Technique for On-Wafer Shield-Based Test Fixtures

Troels Emil Kolding, *Member, IEEE*, and Christian Rye Iversen

***Abstract*—Conventional on-wafer test fixtures have a significant impact on two-port noise-parameter measurements of silicon devices at gigahertz frequencies. This leads to increased measuring inaccuracy, as well as a need for complicated and area-consuming deembedding procedures. Alternatively, shield-based test fixtures are characterized by very few series effects and, thus, support cost-efficient and simple deembedding. The applicability of a simple one-step method is illustrated with experimental data. A performance comparison is made to full-scale deembedding methods based on conventional, as well as shield-based test fixtures.**

***Index Terms*—Integrated circuits, microwave measurements, semiconductor device noise.**

I. Introduction

With the increased application of silicon technology for RF applications, microwave characterization of MOSFETs and bipolar junction transistors (BJTs) has become an important sales parameter for the semiconductor industry; even to those foundries that used to concentrate on digital and low-frequency analog applications. To decrease cost and complexity of device characterization, it is important that simple, yet accurate, measuring approaches become available. In a previous publication [1], it was shown that the use of shield-based on-wafer test fixtures greatly improves the accuracy, as well as the convenience of scattering-parameter measurements. In this paper, we will demonstrate that such test fixtures are also highly applicable to high-frequency noise-parameter measurements.

Conventional test fixtures, as shown in Fig. 1(a), may be characterized by the equivalent test-fixture model shown in Fig. 1(c) [2]. The resistive loss of substrate and series interconnects gives a large discrepancy between raw noise measurements and the actual noise parameters of the device-under-test (DUT). The equivalent series resistance of the parallel effects of conventional test fixtures ($\Re\{Z_p\}$ and $\Re\{Z_d\}$) is often very high; typically 20–100 Ω. This may lead to a significant offset between minimum noise figure $\mathrm{NF}_{\min}$ and equivalent noise resistance R_n between the actual DUT and the DUT measured in a test fixture [3], [4]. Shield-based test fixtures, as shown in Fig. 1(b), have been introduced to reduce the resistive losses of dangling leg straps (Z_s), as well as the coupling parameters Z_p, Z_d, and Z_f [1]. The resistive part of the parallel components is typically below 1 Ω for shield-based implementations, whereas the noise contribution of the test fixture is often low enough to be neglected in comparison to the DUT noise. These considerations allow us to propose and test a simple measuring approach based on shield-based fixtures. In this paper, we will compare a full-scale deembedding (FSD) approach to this simple method in terms of accuracy. As a means of verification, we use measurements of devices and test structures fabricated in a submicrometer CMOS technology.

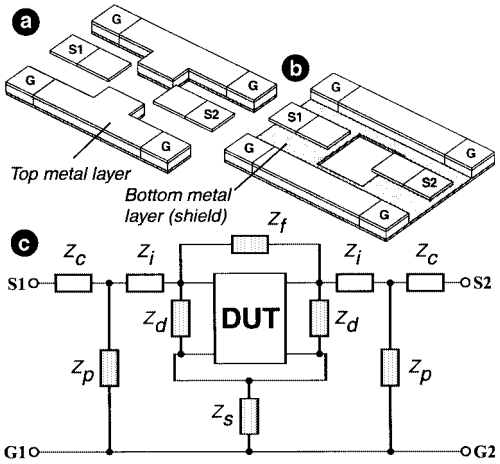

Fig. 1. Illustration of: (a) conventional test fixture, (b) shield-based test fixture, and (c) full-scale equivalent model for fixture parasitics.

II. FSD

The traditional deembedding of noise measurements is based on noise correlation matrices, as proposed by Hillbrand and Russer [5]. The procedure goes through: 1) identification of parasitics and 2) subtraction of these using either cascade, admittance, or impedance representations. The method has been generalized in several references, including [4] and [6]. When using the full-scale equivalent test-fixture model shown in Fig. 1(c), the method becomes quite involved and several on-wafer test structures are required in order to conduct the parasitics extraction. A division of the test-fixture model into convenient parameter groups is depicted in Fig. 2.

We may assume that all model parameters have been determined from an extraction method such as the one presented in [2]. From the total measured noise parameters for the DUT with the test fixture (R_n', $F_{\min}'$, and Y_{SOF}'), we extract the total cascade correlation matrix as [6]

$$\boldsymbol{C}_{A,\,ms} = 2kT_0 \begin{bmatrix} R_n' & \psi^* \\ \psi & R_n'|Y_{\mathrm{SOF}}'|^2 \end{bmatrix} \tag{1}$$

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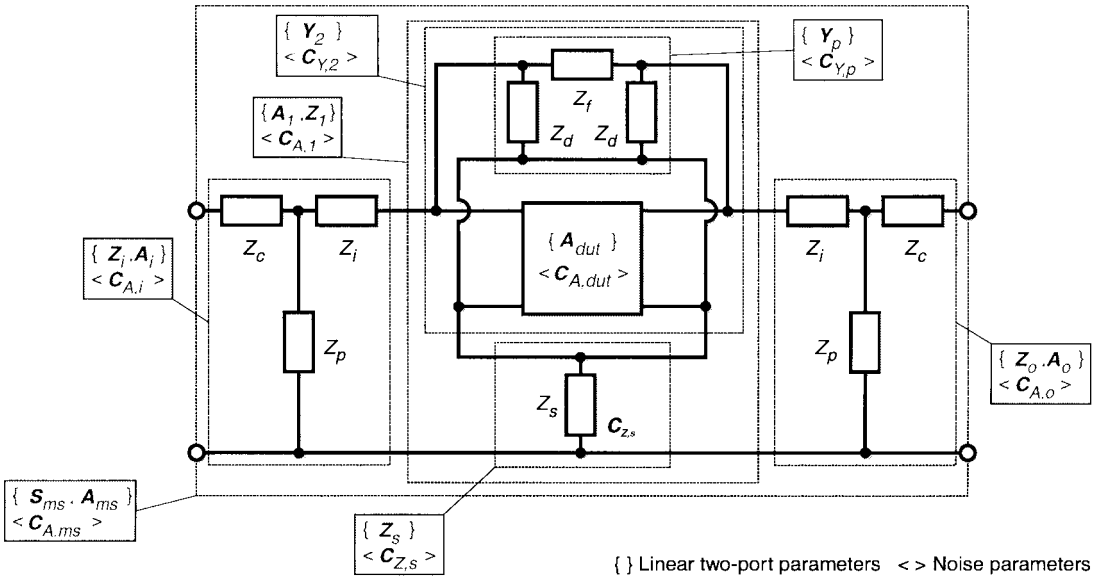

Fig. 2. Redrawn full-scale test-fixture model suitable for noise deembedding. The model is divided into smaller two-port networks that are each characterized by linear two-port parameters, as well as noise correlation matrices.

where

$$\psi = \frac{1}{2}\left(F'_{\min} - 1\right) - R'_n Y'_{\mathrm{SOF}} \tag{2}$$

and T_0 is the standard noise temperature. To simplify the notation, we assume that the noise parameters implicitly refer to the actual noise temperature T_f of the DUT and test fixture. The deembedding procedure starts out by determining the cascade matrix correlation matrices for the input and the output as

$$\boldsymbol{C}_{A,\,i} = 2kT_f \boldsymbol{X}_i \Re\{\boldsymbol{Z}_i\} \boldsymbol{X}_i^{\dagger}, \qquad \boldsymbol{X}_i = \begin{bmatrix} 1 & -1 - \dfrac{Z_c}{Z_p} \\ 0 & -\dfrac{1}{Z_p} \end{bmatrix} \tag{3}$$

$$\boldsymbol{C}_{A,\,o} = 2kT_f \boldsymbol{X}_o \Re\{\boldsymbol{Z}_o\} \boldsymbol{X}_o^{\dagger}, \qquad \boldsymbol{X}_o = \begin{bmatrix} 1 & -1 - \dfrac{Z_i}{Z_p} \\ 0 & -\dfrac{1}{Z_p} \end{bmatrix} \tag{4}$$

where "†" denotes the Hermitian adjoint or complex conjugate transpose given as $\boldsymbol{A}^{\dagger} = (\boldsymbol{A}^T)^*$ [7]. The matrices $\boldsymbol{A}_i$ and $\boldsymbol{A}_o$ can be found using lookup tables found in most microwave textbooks, e.g., [8]. With reference to Fig. 2, we determine the inner cascade correlation matrix as

$$\boldsymbol{C}_{A,\,1} = \boldsymbol{A}_i^{-1}\left(\boldsymbol{C}_{A,\,ms} - \boldsymbol{C}_{A,\,i}\right)\left(\boldsymbol{A}_i^{\dagger}\right)^{-1} - \boldsymbol{A}_1 \boldsymbol{C}_{A,\,o} \boldsymbol{A}_1^{\dagger}. \tag{5}$$

The $ABCD$ two-port matrix $\boldsymbol{A}_1$ is determined from the measured parameters as

$$\boldsymbol{A}_1 = \boldsymbol{A}_i^{-1} \boldsymbol{A}_{ms} \boldsymbol{A}_o^{-1} \tag{6}$$

whereas the input and output two-ports have been removed. To continue the deembedding of Z_s, Z_d, and Z_f, the admittance noise correlation matrix is determined as

$$\boldsymbol{C}_{Y,\,2} = \boldsymbol{Y}_2\Big(\boldsymbol{C}_{Z,\,1} - 2kT_f \Re\{\boldsymbol{Z}_s\}\Big)\boldsymbol{Y}_2^{\dagger} \tag{7}$$

where

$$\boldsymbol{C}_{Z,\,1} = \boldsymbol{X}_1 \boldsymbol{C}_{A,\,1} \boldsymbol{X}_1^{\dagger}, \qquad \boldsymbol{X}_1 = \begin{bmatrix} 1 & -z_{1,\,11} \\ 0 & -z_{1,\,21} \end{bmatrix} \tag{8}$$

where $z_{1,\,rc}$ denotes the element on row r and column c in matrix $\boldsymbol{Z}_1$. The last deembedding step is then conducted as

$$\boldsymbol{C}_{A,\,\mathrm{dut}} = \boldsymbol{X}_{\mathrm{dut}}\Big(\boldsymbol{C}_{Y,\,2} - 2kT_f \Re\left\{\boldsymbol{Y}_p\right\}\Big)\boldsymbol{X}_{\mathrm{dut}}^{\dagger} \tag{9}$$

$$\boldsymbol{X}_{\mathrm{dut}} = \begin{bmatrix} 0 & b_{\mathrm{dut}} \\ 1 & d_{\mathrm{dut}} \end{bmatrix} \tag{10}$$

where a_{dut}, b_{dut}, c_{dut}, and d_{dut} denote the elements of the DUT $ABCD$ matrix $\boldsymbol{A}_{\mathrm{dut}}$. We may then calculate the DUT noise parameters as [6]

$$Y_{\mathrm{SOF}} = \sqrt{\frac{C_{A,\,22}}{C_{A,\,11}} - \left(\frac{\Im\{C_{A,\,12}\}}{C_{A,\,11}}\right)^2} + j\left(\frac{\Im\{C_{A,\,12}\}}{C_{A,\,11}}\right) \tag{11}$$

$$F_{\min} = 1 + \frac{1}{kT_0}\left(C_{A,\,12} + C_{A,\,11} Y_{\mathrm{SOF}}^*\right) \tag{12}$$

$$R_n = \frac{C_{A,\,11}}{2kT_0} \tag{13}$$

which is the desired result. The method may easily be expanded to asymmetrical test fixtures by denoting input and output fixture parasitics separately. Also note that, for shield-based test fixtures, where we may often disregard the parasitics Z_f and Z_s, the last two steps of the deembedding algorithm are greatly simplified.

III. Reduced Complexity Deembedding (RCD)

As noted from the previous section, only the resistive effects of the test fixture are important to the noise correlation matrices. As mentioned previously, the shield-based fixture design method is an effective way of reducing these series parasitics. Hence, we propose a simple noise deembedding technique, which uses no correction of the noise figure and the equivalent noise resistance. However, we compensate for the reactive effects of the test fixture. The method is detailed as follows.

1) Measure the noise parameters ($\mathrm{NF}'_{\min}$, Γ'_{SOF}, and R'_n) with a measuring system calibrated to the probe tips.
2) Approximate the DUT $\mathrm{NF}_{\min}$ and R_n by the measured values $\mathrm{NF}'_{\min}$ and R'_n.
3) Measure the total input admittance of an open test fixture (Y_{open}) and estimate the optimum source reflection as

$$\hat{\Gamma}_{\mathrm{SOF}} = \frac{2\Gamma'_{\mathrm{SOF}} - Y_{\mathrm{open}}Z_0\left(1+\Gamma'_{\mathrm{SOF}}\right)}{2+Y_{\mathrm{open}}Z_0\left(1+\Gamma'_{\mathrm{SOF}}\right)} \tag{14}$$

where Z_0 is the calibration reference impedance.

Hence, the approach requires the fabrication of the test fixture containing the DUT and an additional "open" test fixture. The latter may be obtained simply by separating the DUT from the test fixture using a laser, which may completely alleviate the need for an additional test structure. Although the laser trimming may introduce deembedding imperfections, this effect may be cancelled by the fact that it is the actual test fixture upon which deembedding measurements are being conducted (no tolerances are present).

IV. Experimental Verification

To verify the proposed deembedding method, we have fabricated several test fixtures and devices in standard CMOS silicon technologies employing 10-$\Omega \cdot$ cm substrates. The measurements kit includes deembedding standards needed to conduct the full-scale four-step deembedding method [2], also including the open deembedding standard. The kits are available for a conventional test fixture, as well as a shield-based test fixture (example fixtures are given in Fig. 3). An extracted equivalent model for a typical shielded test fixture is illustrated in Fig. 3(b) with comparison to actual measurements in Fig. 3(d).

Further, the kits include MOSFET devices mounted for two-port measurements in the common-source configuration. The method of verification has been as follows.

1) Using S-parameter measurements on the deembedding standards extract, an equivalent model at all relevant frequencies for the raw test fixtures (conventional, as well as shield-based) was extracted, e.g., [9].
2) Noise measurements were conducted on the DUT at various frequencies and the noise parameters for the DUT with the test fixture extracted.
3) Using the extracted test-fixture model, as well as the noise measurement results, the intrinsic DUT noise parameters are extracted using the two noise deembedding methods outlined earlier. The measurement setup includes a vector network analyzer, a probe station mounted with ground–signal–ground microwave probes, as well as impedance tuners for reporting the noise parameters at various source settings.

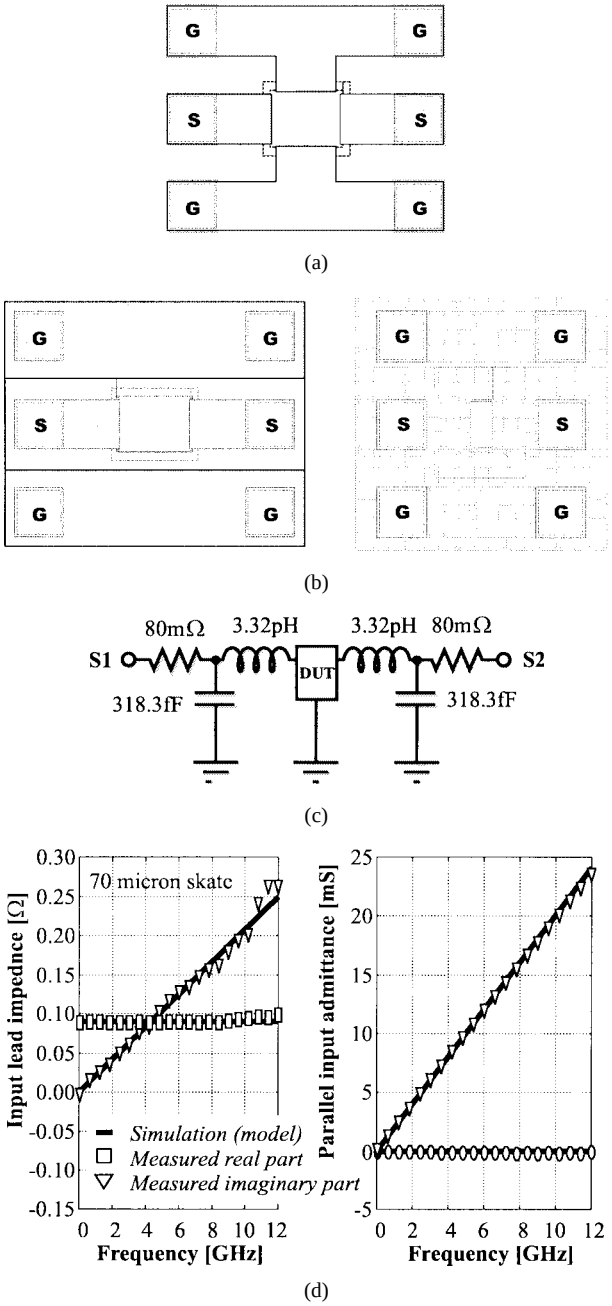

Fig. 3. Illustration of: (a) conventional and (b) shield-based test fixtures used in this study. In (c), a typical model for a shield-based test fixture is shown with comparison to its measured response in (d). All test fixtures employ a 150-μm pad–pad spacing. Other implementation details can be found in [1] and [9].

The raw noise measurements of the DUT including a test fixture, as well as the deembedded results using the FSD and RSD methods, are listed in Table I for various scenarios (two different RF-optimized MOSFETs in two different CMOS technologies). We shall assume the FSD results to serve as a reasonable reference, as this method uses an accurately extracted

TABLE I
NOISE PARAMETERS FOR THE DUT WITH A TEST FIXTURE, DUT ESTIMATED WITH FSD, AND DUT ESTIMATED WITH RSD. MEASUREMENTS WITH A CONVENTIONAL TEST FIXTURE ARE DENOTED BY "CNV," WHILE MEASUREMENTS WITH A SHIELD-BASED TEST FIXTURE ARE DENOTED BY "SHL"

NMOS DUT	Fixt. type	Raw measurement			FSD			RSD		
		NF_{min} [dB]	R_n [Ω]	Γ_{SOF} [-,deg]	NF_{min} [dB]	R_n [Ω]	Γ_{SOF} [-,deg]	NF_{min} [dB]	R_n [Ω]	Γ_{SOF} [-,deg]
300x0.5μm, 1.6GHz	Cnv.	1.27	75.8	0.799∠44.5°	1.05	76.0	0.810∠33.0°	1.27	75.8	0.780∠34.3°
300x0.5μm, 1.6GHz	Shl.	1.08	75.8	0.816∠43.4°	1.05	75.9	0.811∠33.0°	1.08	75.8	0.806∠33.1°
400x0.25μm, 1.6GHz	Shl.	0.57	20.0	0.639∠60.9°	0.54	19.6	0.722∠30.7°	0.57	20.0	0.713∠30.8°
400x0.25μm, 2.1GHz	Shl.	0.76	18.0	0.639∠60.9°	0.70	17.6	0.637∠54.6°	0.76	18.0	0.623∠54.8°
400x0.25μm, 2.7GHz	Shl.	0.86	17.5	0.640∠71.2°	0.78	17.1	0.633∠63.8°	0.86	17.5	0.617∠64.3°

Measuring temperature is 25°C.

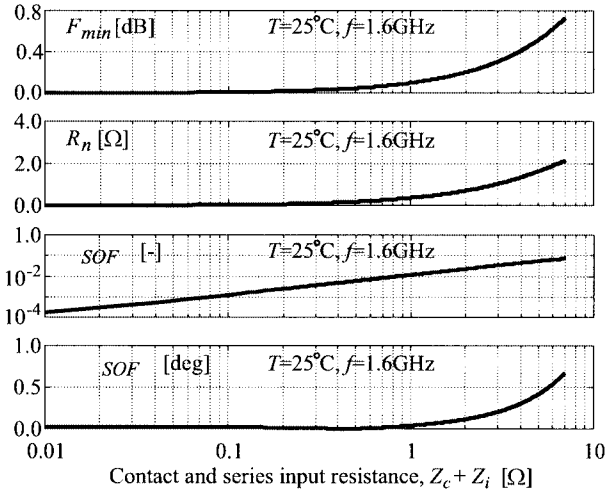

Fig. 4. Impact of series effects on noise parameters of 300 × 0.5 μm NMOS. For the given case, we assume $\Im\{Z_c + Z_i\} = 1.4\Re\{Z_c + Z_i\}$.

test-fixture model and a proven deembedding technique. Generally, the influence of the shield-based fixture on $\mathrm{NF_{min}}$ is very small with distortion of only 0.03, 0.06, and 0.08 dB at 1.6, 2.1, and 2.7 GHz, respectively. This is close to the specified measuring uncertainty of our system. In comparison, the conventional fixture leads to a rise in $\mathrm{NF_{min}}$ of 0.22 dB at 1.6 GHz. The influence on R_n is, in both cases, small. For both test fixtures, it is observed that $|\Gamma_{\mathrm{SOF}}|$ is only slightly affected, while $\angle\Gamma_{\mathrm{SOF}}$ is affected considerably.

For the shield-based test fixtures, the proposed one-step deembedding method (i.e., RSD) effectively estimates the device Γ_{SOF}. It is, however, interesting to note that, in some cases, the raw measured reflection $|\Gamma'_{\mathrm{SOF}}|$ is closer to the device $|\Gamma_{\mathrm{SOF}}|$ than the deembedded reflection $|\hat{\Gamma}_{\mathrm{SOF}}|$. This is caused by two counteracting effects, i.e., a reduction of $|\Gamma_{\mathrm{SOF}}|$ due to the parallel admittance of the fixture and an increase of $|\Gamma_{\mathrm{SOF}}|$ due to thermal noise generated in the input series parasitics. The proposed method compensates only for the parallel admittance and, thus, slightly underestimates $|\Gamma_{\mathrm{SOF}}|$.

The sensitivity of the proposed deembedding method (i.e., RSD) versus the value of the input series effects $Z_c + Z_i$ is plotted in Fig. 4. If the series effects are kept well below 1 Ω, the impact on the noise parameters is typically negligible. This requirement can be fulfilled in most silicon processes, even when including the contact resistance between probes and aluminum metallization.

V. CONCLUSIONS

In this paper, we have derived an FSD technique compatible with the four-step deembedding model. Further, a simple one-step correction procedure has been proposed for device noise measurements utilizing shield-based test fixtures. Correction is applied for the parallel test-fixture admittance, which is easily estimated with an additional open test fixture. When input series parasitics of the test fixture are kept well below 1 Ω, measuring errors on the noise parameters are close to the overall measuring uncertainty. Using the simple one-step method, one can expect typical noise-figure accuracy better than 0.05 dB and a noise-resistance accuracy better than 0.1–0.2 Ω. For more critical cases, e.g., when device noise is very low or the measuring frequency is very high, a full deembedding method should be used. This requires an additional fully shorted test dummy structure. Due to low noise contribution of the shield-based test fixture, the measuring accuracy is generally improved over conventional fixtures. For more critical cases, e.g., when device noise is very low or the measuring frequency is very high, a full deembedding method can be used.

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